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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,084	07/07/2003	Salvatore Lombardo	856063.547D1	7985

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,084	LOMBARDO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/087,398.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. The restriction requirement set forth in previous office action has been withdrawn.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Reference "xx" shown in fig. 1 is not mentioned in the description. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by admitted prior art ("APA").

The APA discloses in figs. 1 and 3 a heterostructure bipolar transistor, comprising: a substrate comprised of a first semiconductor material doped with impurities of a first type, the substrate including a first conducting region 5; a heterostructure alloy region positioned in the substrate and comprised of a heterostructure alloy of atoms of the first semiconductor material and atoms of a second semiconductor material (figs. 3A and 3B); a base region 3 positioned in the substrate above the first conducting region and doped with impurities of a second type; a first dielectric layer 12 positioned on the substrate/ directly contacting the heterostructure alloy of the of the heterostructure alloy region (as in claim 2), the first dielectric layer defining a first window directly above the heterostructure alloy region; a second conducting region 4 positioned in the heterostructure alloy region and between the first window and the base region, the second conducting region being comprised of the heterostructure alloy doped with impurities of the first type; and a contact region 7 positioned in the first window and comprised of the first semiconductor material, the contact region directly contacting the heterostructure alloy of the second conducting region in the heterostructure alloy region.

As for claim 3, the APA discloses a protective layer 11 positioned over the semiconductor substrate and defining a second window above the heterostructure alloy region, the first dielectric layer being positioned in the second window between the protective layer and the first window.

As for claim 4, the APA discloses a second dielectric layer 14 positioned on the first dielectric layer and in the second window between the protective layer and the first window.

As for claim 5, the APA discloses the first dielectric layer being silicon dioxide and the second dielectric layer being silicon nitride.

As for claim 6, the APA discloses the first semiconductor material being silicon, the second semiconductor material being germanium.

As for claim 7, the APA discloses a metal contact 8 formed directly on the contact region.

5. Claims 8-13 are rejected under 35 U.S.C. 102(b) as being anticipated by APA.

The APA discloses a heterostructure bipolar transistor, comprising: a substrate comprised of a first semiconductor material doped with impurities of a first type, the substrate including a first conducting region 5; a heterostructure alloy region positioned in the substrate and comprised of a heterostructure alloy of atoms of the first semiconductor material and atoms of a second semiconductor material (fig. 3A); a base region 3 positioned in the substrate above the first conducting region and doped with impurities of a second type; a first dielectric layer 12 positioned on, and directly contacting, the heterostructure alloy region, the first dielectric layer defining a first window directly above the heterostructure alloy region; and a second conducting region 4 positioned in the heterostructure alloy region and between the first window and the base region, the second conducting region being comprised of the heterostructure alloy doped with impurities of the first type and directly contacting the first dielectric layer.

As for claim 9, the APA discloses a protective layer 11 positioned over the semiconductor substrate and defining a second window above the heterostructure alloy region, the first dielectric layer being positioned in the second window between the protective layer and the first window.

As for claim 10, the APA discloses a second dielectric layer 14 positioned on the first dielectric layer and in the second window between the protective layer and the first window.

As for claim 11, the APA discloses the first dielectric layer being silicon dioxide and the second dielectric layer being silicon nitride.

As for claim 12, the APA discloses the first semiconductor material being silicon, the second semiconductor material being germanium.

As for claim 13, the APA discloses a contact region 7 positioned in the first window and comprised of the first semiconductor material, the contact region directly contacting the heterostructure alloy of the second conducting region in the heterostructure alloy region; and a metal contact 8 formed directly on the contact region.

6. Claims 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by APA.

The APA discloses a vertical structure high carrier mobility bipolar transistor, comprising substrate of crystalline silicon doped with impurities of the N type, having a collector region 2 located at a lower portion of the substrate, the transistor being obtained by a process that includes: defining a window above the substrate; providing a first implantation of germanium atoms through said window into the substrate; providing a second implantation of acceptor dopants through said window to define a base region in the substrate (figs. 3A and 3B); applying an RTA treatment, or treatment in an oven, to re-construct a crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy; forming a first thin dielectric layer 12 of silicon dioxide on the substrate; depositing a second dielectric layer 14 or silicon nitride (as in claim 17) onto said first dielectric layer; depositing a polysilicon layer 15 onto said second dielectric layer; etching away, within the window region, said first and second dielectric layers, and the polysilicon layer, to expose the base region and form isolation spacers

at edges of the window (fig. 3D); and forming an N-doped emitter 4 directly contacting the first dielectric layer (as in claim 18) in the base and window regions.

As to the formation of said first thin dielectric by chemical vapor deposition or carried out by an atmospheric pressure chemical vapor deposition process or said deposition being followed by thermal deposition recited in claims 14-16 respectively, it refers to a process and "product by process" claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1924.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
November 5, 2004